METHOD AND APPARATUS FOR TESTING A CAM ADDRESSED CACHE

BACKGROUND

Cross Reference to Related Application

[0001] This is a continuation of a pending divisional patent application, Serial No. 10/261,395, filed September 30, 2002, entitled, METHOD AND APPARATUS FOR TESTING A CAM ADDRESSED CACHE which is a divisional of issued Patent No. 6,487,131, issued November 26, 2002 and entitled METHOD AND APPARATUS FOR TESTING A CAM ADDRESSED CACHE.

now US patent No. 6,744,655

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Field of the Invention

[0002] The invention relates to testability. More specifically, the invention relates to testability of content addressable memory.

Background

[0003] Content addressable memory (CAM) addressed caches have gained increasing popularity for use in microprocessor caches. This popularity increase is primarily due to the elimination of the need for a final decode and that such caches permit high set associativity and low power consumption at the expense of some added chip area. Unfortunately, such CAM addressed caches create testing problems because neither the SRAM portion of the array, nor the CAM locations, are directly addressable. In fact, each CAM cell is formed with several transistors, but the only output is a match line indicating match or no match. A match is determined by whether any cell in the row of the match line drives the match line. Thus, CAM testing necessitates developing a scheme whereby only a single column and row are tested at any one time. It may not be possible to develop an algorithmic scheme for such testing and, in any event, such testing would be prohibitively expensive and time consuming for mass marketed components.